P58

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte V. THOMAS POWELL,
ANTON GOEPPEL, GERHARD ROEHRL
and
EDWARD C. KING

Appeal No. 95-1152
Application 07/752,710[1]

ON BRIEF

Before HAIRSTON, KRASS and BARRETT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 20, constituting all the claims in the application.

[1] Application for patent filed August 30, 1991.

The invention pertains to an interface circuit for transferring data words between two busses. More particularly, the circuit allows data words to be transferred out in a different order than they are transferred in.

Representative independent claims 1 and 20 are reproduced as follows:

1. An interface circuit for transferring data words between first and second buses, comprising:

a buffer having a plurality of registers;

write means, connected to said buffer, for storing data words received from said second bus in said registers; and

read means, connected to said buffer, for transferring data words from said registers to said first bus;

wherein each data word is stored in only one register in said buffer, and the order in which the data words are written into said buffer is different than the order in which they are read out of said buffer.

20. A method for transferring a sequence of data words from a first data bus through a buffer to a second data bus comprising:

sorting data words received from said first bus;

storing said words in said buffer; and

transferring said data words, in their sorted order, from said buffer to said second bus.

The examiner relies on the following references:

Utsumi et al. (Utsumi)	4,931,925	June 5, 1990
Taniai et al. (Taniai)	5,043,935	Aug. 27, 1991
Dieffenderfer et al. (Dieffenderfer)	5,224,213	June 29, 1993 (filed Sept. 5, 1989)

Claims 1 through 20 stand rejected under 35 U.S.C. § 102(e) as anticipated by Dieffenderfer.[2] In new grounds of rejection entered by the examiner in the answer, claim 19 now stands rejected under 35 U.S.C. § 112, second paragraph; claims 1 through 9, 12 through 15 and 17 through 20 stand rejected under 35 U.S.C. 102(e) as anticipated by Taniai; and claims 10, 11 and 16 stand rejected under 35 U.S.C. § 103 as unpatentable over Taniai in view of Utsumi.

Reference is made to the briefs and answer for the respective details of the positions of appellants and the examiner.

OPINION

Turning first to the rejection of claim 19 under 35 U.S.C. § 112, second paragraph, the examiner complains about the use of the term "providing." At the bottom of page 6 of the answer, the examiner states, in toto:

> As per claim 19, "providing" is not a physical step in a method claim. Applicant must set forth the actual step being performed, such as generating, inputting, outputting, etc.

[2] The final rejection of claims 1 through 10 under 35 U.S.C. § 112, second paragraph, has been withdrawn by the examiner and is not before us in this appeal.

This rejection is so unreasonable that it is difficult to believe that the examiner is really serious. Perhaps there is something else about the claim which bothers the examiner but which the examiner is having trouble explaining. In any event, "providing" is clearly a proper step in a method claim and there is nothing vague or indefinite about the use of such term. We will not sustain the rejection of claim 19 under 35 U.S.C. § 112, second paragraph.

Turning now to the prior art rejections, we will sustain the rejection of claim 20 under 35 U.S.C. § 102(e) as anticipated by Dieffenderfer but we will not sustain any of the other prior art rejections.

Each of claims 1 through 19 requires that "the order in which the data words are written into said buffer is different than the order in which they are read out of said buffer."

Dieffenderfer discloses a ping-pong data buffer wherein data is read from a storage array and supplied to one data bus simultaneously with the writing of data into the array from another data bus. At column 9, lines 39-48, of Dieffenderfer, it is stated:

> The read and write functions of the lower and upper portions 41 and 42 of the storage

> array 26 are interchanged back in [sic, and] forth from time to time so that data from one of the data buses is written into the lower portion 41 and then the upper portion 42 in an alternating manner while data that is read out and supplied to the other data bus is read from the upper portion 42 and then the lower portion 41 in an alternating manner which is the opposite of that used for the writing of data into the storage array 26.

While this portion of the reference's disclosure indicates that a writing and reading function are "opposite," it refers to the nature of the write/read operation regarding whether the lower or the upper portion of the storage array is being read from or written to. While it may very well be that the order in which data words are read from the storage array is different than the order in which they are written into the storage array, there is absolutely no disclosure in Dieffenderfer that the order is different. A proper anticipation rejection under 35 U.S.C. § 102 requires that the examiner point out how each and every one of the claimed elements and limitations is taught by the applied reference. While the examiner has pointed to column 5 and column 9, lines 39-54, of Dieffenderfer [see page 3 of the answer] for the different order limitation, we do not find such a teaching therein and we decline to engage in speculation in order to provide the deficiency.

Accordingly, we will not sustain the rejection of claims 1 through 19 under 35 U.S.C. § 102(e) as anticipated by Dieffenderfer.

In a new ground of rejection, the examiner relies on Taniai as an anticipatory reference regarding claims 1 through 9, 12 through 15 and 17 through 20. The problem with this rejection is that it is not clear how the examiner is interpreting the reference with regard to the first and second bus and with regard to the claimed different order.

In the application of the rejection, at page 7 of the answer, the examiner says nothing about a first and second bus. Further the claimed different order is said to be disclosed in Taniai in the "abstract, figure 1, and column 3, lines 31-65, his swap circuit."

Since this was a new ground of rejection, appellants filed a reply brief in response to the rejection and argued that the examiner did not identify first and second buses in Taniai, stating that Taniai discloses only a single bus 1. Appellants even speculated that perhaps the examiner meant to point to one of the bus lines 1a-1d as a "first bus" and others as a "second bus." With regard to the claimed order, appellants argued that although Taniai changes the alignment of bytes, there is no

disclosure of a changing of the order in which the bytes are transferred.

The examiner's response to these arguments was to say absolutely nothing. Therefore, we have nothing in the record indicating the examiner's position on these points. On the other hand, we have appellants' arguments which appear to have some merit in view of the disclosure of Taniai. While Taniai discloses "rearranging a data arrangement of the data received from the source . . ." [abstract], and Figures 4 and 5 appear to indicate some change in alignment of data, we find nothing, and the examiner has not convincingly pointed to anything, in Taniai which teaches that the order of data words written into a buffer is different than the order in which they are read out of the buffer.

Since appellants have made a reasonable argument and the examiner never set forth a position on these arguments, we will not sustain the rejection of claims 1 through 9, 12 through 15 and 17 through 20 under 35 U.S.C. § 102(e) over Taniai and we will also not sustain the rejection of dependent claims 10, 11 and 16 under 35 U.S.C. § 103 over Taniai in view of Utsumi since Utsumi fails to provide for the deficiencies noted supra with regard to Taniai.

With regard to claim 20, while we have not sustained the rejection of this claim over Taniai because the examiner has failed to identify the first and second bus in Taniai on which he relies, we will sustain the rejection of claim 20 under 35 U.S.C. § 102(e) over Dieffenderfer because the claimed subject matter therein is of such a broad nature as to read on the disclosure of Dieffenderfer.

More particularly, claim 20 does not require that the order of data words written into a buffer be different than the order from which they are read out of the buffer. It requires only "sorting" data words received from the first bus, storing the words and transferring the words, "in their sorted order," to the second bus. This language is broad enough, in our view, to include the situation where the incoming data words are "sorted" so as to be in the same order as received on the first bus, i.e., no change is also a "sort."

In such a situation, the sequence of data words received on the first bus is simply stored in a buffer and subsequently transferred, in that sequence, to the second bus. This reasonable interpretation of the language of claim 20 clearly reads on the disclosure of Dieffenderfer.

We have not sustained the rejection of claim 19 under 35 U.S.C. § 112, second paragraph. We also have not sustained

the rejection of claims 1-9, 12-15 and 17-20 under 35 U.S.C. § 102(e) over Taniai or of claims 10, 11 and 16 under 35 U.S.C. § 103 over Taniai in view of Utsumi. We have, however, sustained the rejection of claim 20 under 35 U.S.C. § 102(e) as anticipated by Dieffenderfer.

Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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ERROL A. KRASS) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
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